ML1001D Series Static LCD COG Driver

❖ *Application*

- *Instrument LCD Module*
- *Telephone LCD Module*
- *Automotive LCD Module*
- *Handheld Device LCD Module*

❖ *Features*

- A Gold Bump Chip without external component.
- Logic & LCD power supply: 2.0V to 6.0V
- Typical Current consumption: 25uA at V_{IN} = 3V & no load condition.
- Number of segments: 40
- Cascade the ML1001 to form a single piece of 80 or 120 segments LCD driver.
- Simple 3 pin microcontroller interface through DIN, DCLK & LOAD.
- Blink of the display data.
- Offer best contrast and widest viewing angle of TN LCD technology.
- No temperature compensation needed for Topr = -40°C to 80°C.

❖ *General Description*

ML1001D static LCD COG (chip on glass) driver is 40 segments LCD driver with gold bump. It can be cascaded to form a single piece of 80 or 120 segments LCD drivers. It targets at custom TN LCD COG Module product which requires the best quality of TN LCD technology. With the use of ML1001 series driver, it offers the best contrast, the widest viewing angle, the widest range of operating voltage and the widest range of operating temperature when compared to the multiplex method.

Our ML1001D includes an internal 32kHz oscillator, a 40-bit shift register, a 40-bit data register, a 16-bit segment driver, a 24-bit segment driver, two common drivers, a blink control circuit, a power-up reset circuit and a frequency divider which offer the necessary clock signals for Blink control, segment & common driver circuit.

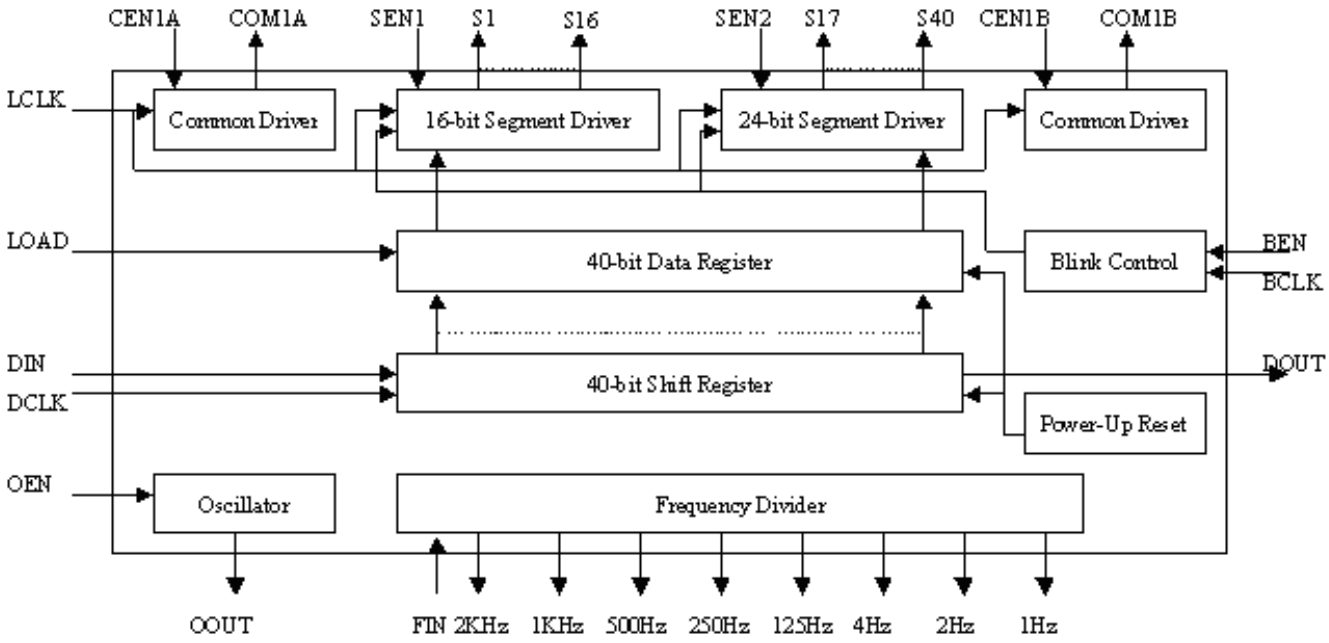
Through the DIN pin, the display data is serially shifted into the 40-bit shift register at the rising edge of DCLK signal. The display data, which is going to be displayed on the attached LCD, is then stored in the 40-bit data register at the rising edge of the LOAD signal.

Other features like blinking of the display data by the BEN and BCLK, disable the internal oscillator by the OEN, input an external clock signal to the FIN, and enable or disable the segment and common driver by the SEN1, SEN2, CEN1A and CEN1B, are included.

❖ *Ordering Information*

Part Number	Description	Package Form
ML1001D-1U	a 40 segment static LCD driver	Gold Bump Die
ML1001D-2U	a 80 segment static LCD driver	Gold Bump Die
ML1001D-3U	a 120 segment static LCD driver	Gold Bump Die

❖ *Block Diagram*



❖ *Absolute Maximum Ratings*

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply voltage	V_{DD}		-0.5	+7.0	V
Supply Current	I_{DD}	V_{DD} = 3V, no Load	-50	+50	mA
Input Voltage	V_{IN}		GND-0.3	V_{DD} +0.3	V
Output Voltage	V_{OUT}		GND-0.3	V_{DD} +0.3	V
DC input Current	I_{IN}		-10	+10	mA
DC output Current	I_{OUT}		-10	+10	mA
Storage temperature	T_{stg}		-65	+150	^{o}C
Total power dissipation	P_{tot}		-	400	mW

❖ *DC Characteristic*

V_{DD} = 3.0V; T_{amb} = 25°C ; unless otherwise specified

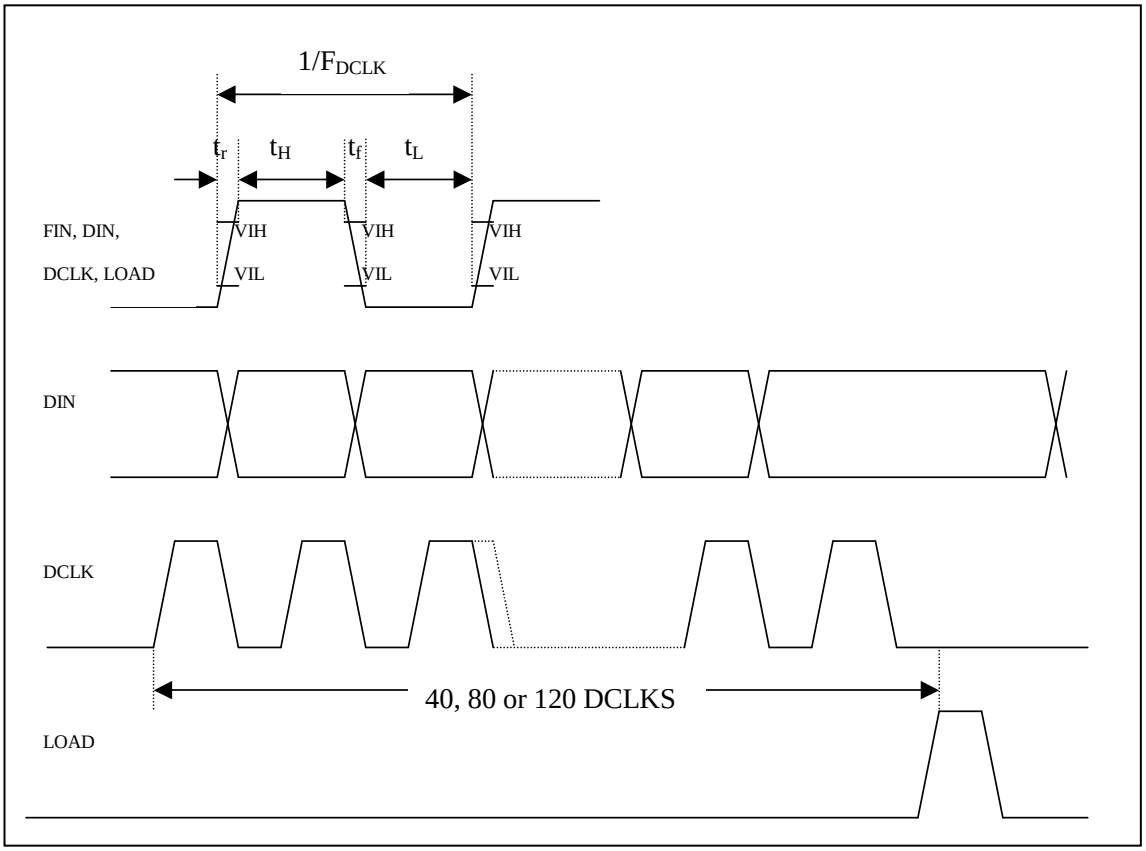
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supplies						
Supply voltage	V_{DD}		2.0	-	6.0	V
Supply Current	I_{DD}	Disable Oscillator	-	0.1	0.5	uA
Supply Current	I_{DD}	Enable Oscillator	-	25	60	uA
Logic						
LOW-level input voltage	V_{IL}		GND	-	$0.3*V_{DD}$	V
HIGH-level input voltage	V_{IH}		$0.7*V_{DD}$	-	V_{DD}	V
LOW-level output current	I_{OL}	V_{OL} = 1.0V	1	-	-	mA
HIGH-level output current	I_{OH}	V_{OH} = 2.0V	-1	-	-	mA
LCD outputs						
Output resistance at pads S1 to S40	R_{SEG}		-	85	150	ohm
Output resistance at pads COM1A and COM1B	R_{COM}		-	45	100	ohm

❖ *AC Characteristic*

V_{DD} =3.0V; T_{amb} = 25°C; unless otherwise specified

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillator frequency at pad OOUT	f_{oout}		21	32	48	kHz
FIN, LOAD, DIN, DCLK High time	t_H		0.4	-	-	us
FIN, LOAD, DIN, DCLK Low time	t_L		0.4	-	-	us
FIN, LOAD, DIN, DCLK Rise time	t_r		-	-	10	us
FIN, LOAD, DIN, DCLK Fall time	t_f		-	-	10	us
DCLK Frequency	F_{DCLK}		1	-	100	kHz
Baudrate	Bps_{DCLK}		1	-	500	kbps

❖ *Timing Diagram*



❖ *Functional Description*

The ML1001D is a static LCD COG (chip on glass) driver which can drive upto 40 segments or cascaded with two or three ML1001s to drive 80 & 120 segments. There is a shift register for serially shifting in the data and a data register to store the data that is going to be displayed. The display data is read into the shift register serially through the DIN pin at the rising edge of the DCLK signal. The display data will then be displayed at the rising edge of the LOAD signal. The display data in the shift register is output by the DOUT pin after 40 rising edges of the DCLK signal. The display data should be input in the sequence of SEG40, SEG39… SEG2, SEG1 for proper display of data.

i) Power on reset

At Power on the ML1001 resets to a starting condition as follows:

1. The shift register outputs are set to GND.
2. The data register outputs are set to GND, hence all LCD segments off.

ii) Oscillator

a) Internal clock
The internal logic and the LCD driving signal of ML1001 are clocked either by the built-in oscillator or from an external clock. When the internal oscillator is used, OEN should be connected to GND and the OOUT should be connected to FIN. The oscillator will oscillate at 32 kHz and the frequency is independent in the range of $2.0V \leq V_{DD} \leq 6.0V$.

b) External clock
When using an external clock, the OEN is connected to VDD then connects the external clock to FIN.

iii) Timing

ML1001D have several frequencies of clock signal for the users to choose for the LCD display clock (ie. LCLK) and the blink clock (ie. BCLK). They include the following clock signals :

Frequency of Clock Signal at FIN = 32 kHz	Actual Divider of FIN	Target Input Pin
2 KHz	1/16	LCLK
1 KHz	1/32	
500 Hz	1/64	
256 Hz	1/128	
128 Hz	1/256	
4 Hz	1/8192	BCLK
2 Hz	1/16384	
1 Hz	1/32768	

iv) Segment outputs

ML1001D has 40 segment outputs which should be connected directly to the LCD. If less than 40 segments are required, the unused segments should be left open circuit. Users can disable the first 1 to 16 segments and the last 17 to 40 segments by connecting the SEN1 and SEN2 to VDD, respectively. The segment outputs shall output GND level after disabling it.

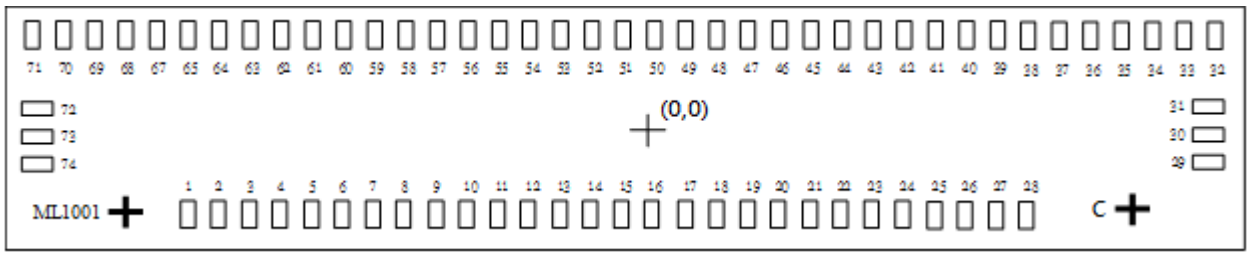
v) Common outputs

ML1001D consists of 2 common signals (ie. COM1A & COM1B). These two common signals are the inversion of the LCLK. The common outputs should be left open-circuit if the outputs are unused. Users can disable the COM1A and COM1B by connecting the CEN1A and CEN1B to VDD, respectively. The common outputs will change to GND after disabling it.

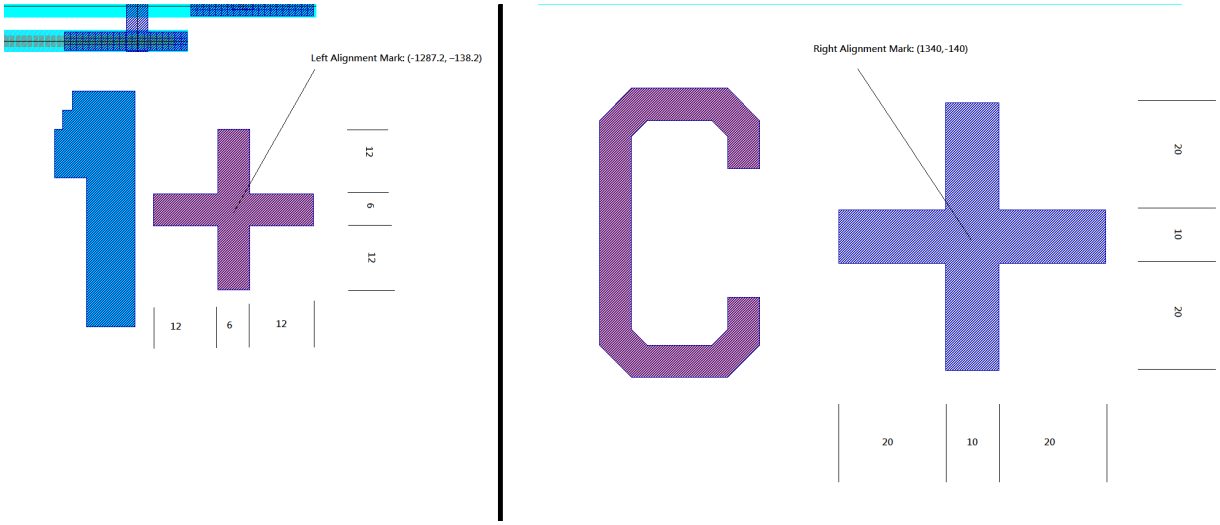
vi) Blink

ML1001D has a blink function that users shall connect the BEN to GND and input the blink clock (ie. BCLK) either by connecting ML1001 output clock signal from Frequency Divider or an external clock signal. Users shall disable blink function by connecting BEN to VDD.

❖ *Pad Configuration*



Alignment Mark:



Chip Size :

Part Number	Description	Chip Size
ML1001D-1U	a 40 segment static LCD driver	3,440 um x 600 um
ML1001D-2U	a 80 segment static LCD driver	6,880 um x 600 um
ML1001D-3U	a 120 segment static LCD driver	10,320 um x 600 um

Chip Thickness : 400 um ± 25 um
Gold Bump Pad Size : 32 um x 72 um
Gold Bump Height : 18 um ± 2 um
Right Alignment mark : (1340, -140)
Left Alignment mark : (-1287.2, -138.2)
Origin on the center of ML1001 IC

Note :
1. The die faces up in the diagram.

❖ *Pad Location*

All x and y coordinates are references to the center of the chip.

PAD	PAD	Coordinate		PAD	PAD	Coordinate		PAD	PAD	Coordinate	
Num.	Name	X	Y	Num.	Name	X	Y	Num.	Name	X	Y
1	LOAD	-1246	-140	26	DCLK	1054	-140	51	S21	20	140
2	DIN	-1146	-140	27	DOUT	1134	-140	52	S20	-60	140
3	DCLK	-1046	-140	28	LOAD	1234	-140	53	S19	-140	140
4	BEN	-946	-140	29	GND	1560	-120	54	S18	-220	140
5	OEN	-846	-140	30	VDD	1560	-40	55	S17	-300	140
6	VDD	-746	-140	31	COM1B	1560	40	56	S16	-380	140
7	SEN1	-666	-140	32	S40	1540	140	57	S15	-460	140
8	CEN1A	-566	-140	33	S39	1460	140	58	S14	-540	140
9	SEN2	-466	-140	34	S38	1380	140	59	S13	-620	140
10	CEN1B	-366	-140	35	S37	1300	140	60	S12	-700	140
11	GND	-266	-140	36	S36	1220	140	61	S11	-780	140
12	OOUT	-186	-140	37	S35	1140	140	62	S10	-860	140
13	FIN	-86	-140	38	S34	1060	140	63	S9	-940	140
14	LCLK	14	-140	39	S33	980	140	64	S8	-1020	140
15	2 KHz	94	-140	40	S32	900	140	65	S7	-1100	140
16	1 KHz	174	-140	41	S31	820	140	66	S6	-1180	140
17	500 Hz	254	-140	42	S30	740	140	67	S5	-1260	140
18	250 Hz	334	-140	43	S29	660	140	68	S4	-1340	140
19	125 Hz	414	-140	44	S28	580	140	69	S3	-1420	140
20	4 Hz	494	-140	45	S27	500	140	70	S2	-1500	140
21	2 Hz	574	-140	46	S26	420	140	71	S1	-1580	140
22	1 Hz	654	-140	47	S25	340	140	72	COM1A	-1560	40
23	BCLK	754	-140	48	S24	260	140	73	VDD	-1560	-40
24	LCLK	854	-140	49	S23	180	140	74	GND	-1560	-120
25	BEN	954	-140	50	S22	100	140				

❖ *Pin Description*

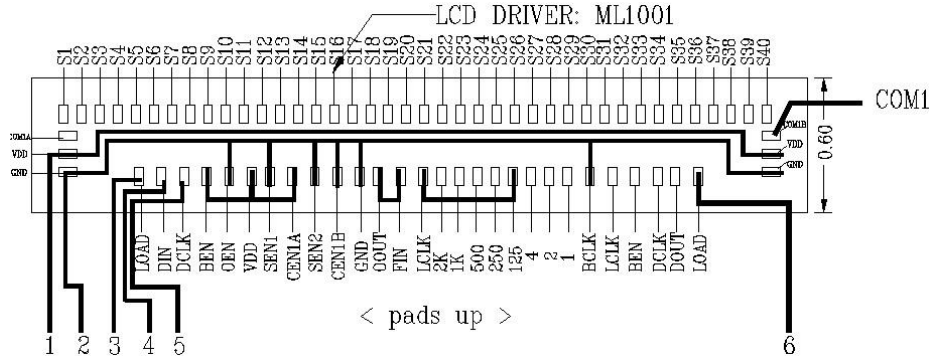
Symbol	Pad	Description
LOAD	1,28	Load data from the shift register to data register; note 1
DIN	2	Display data input pin
DCLK	3,26	Input pin for the clock of the display data; note 1
BEN	4,25	Enable pin of the blink function; note 1, note 2
OEN	5	Enable pin of the internal oscillator; note 2
V_{DD}	6	Supply voltage
SEN1	7	Enable pin of the segment from S1 to S16; note 1
CEN1A	8	Enable pin of the COM1A; note 2
SEN2	9	Enable pin of the segment from S17 to S40; note 1
CEN1B	10	Enable pin of the COM1B; note 2
GND	11	Logic ground
OOUT	12	Output pin of the internal oscillator
FIN	13	Input pin of the external/internal clock
LCLK	14,24	Input pin to the LCD display clock; note 1
2 kHz	15	Output 1/16 frequency of the input to the FIN; note 3
1 kHz	16	Output 1/32 frequency of the input to the FIN; note 3
512 Hz	17	Output 1/64 frequency of the input to the FIN; note 3
256 Hz	18	Output 1/128 frequency of the input to the FIN; note 3
128 Hz	19	Output 1/256 frequency of the input to the FIN; note 3
4 Hz	20	Output 1/8192 frequency of the input to the FIN; note 3
2 Hz	21	Output 1/16384 frequency of the input to the FIN; note 3
1 Hz	22	Output 1/32768 frequency of the input to the FIN; note 3
BCLK	23	Input pin for the blink clock
DOUT	27	Output pin for 40-bit Shift register, it shall connect to DIN of next ML1001
GND	29	Logic ground
V_{DD}	30	Supply voltage
COM1B	31	Common driving signal to LCD panel
S40 to S1	32 to 71	LCD segment outputs
COM1A	72	Common driving signal to LCD panel
V_{DD}	73	Supply voltage
GND	74	Logic ground

Note :

1. *In cascade format of ML1001D (ie. ML1001D-2U and –3U), one pin is the input of current ML1001D and the other is for the connection with the corresponding input pin of next ML1001D.*
2. *All Enable pins are active low.*
3. *Condition : FIN = 32 KHz Clock.*

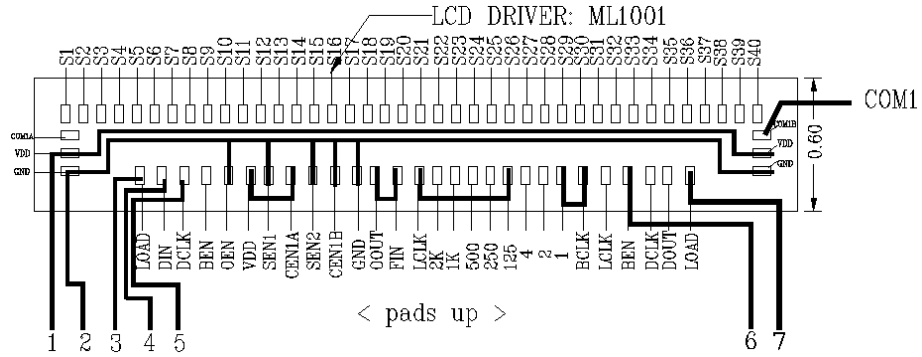
❖ *Application Examples*

ML1001D-1U Standard Application



Pin	Pin Name
1	VDD
2	GND
3	LOAD
4	DIN
5	DCLK
6	CHECK

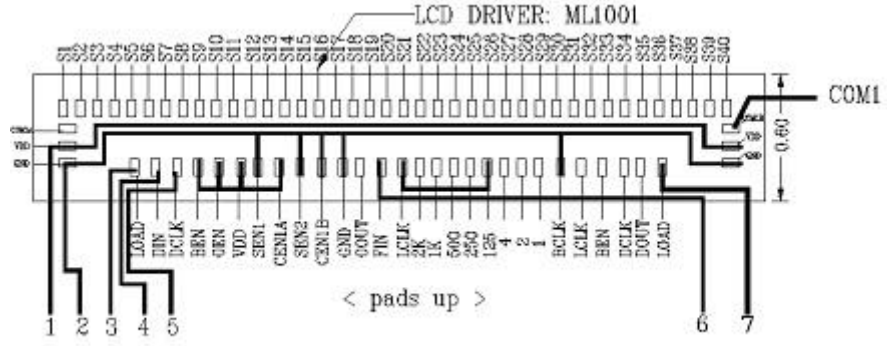
ML1001D-1U Application Circuit with 1 Hz Blink Feature



Pin	Pin Name
1	VDD
2	GND
3	LOAD
4	DIN
5	DCLK
6	BEN
7	CHECK

Note : Blink at 1 Hz if BEN = 0V, Normal Display if BEN = VDD.

ML1001D-1U Application Circuit with External 32 KHz Clock

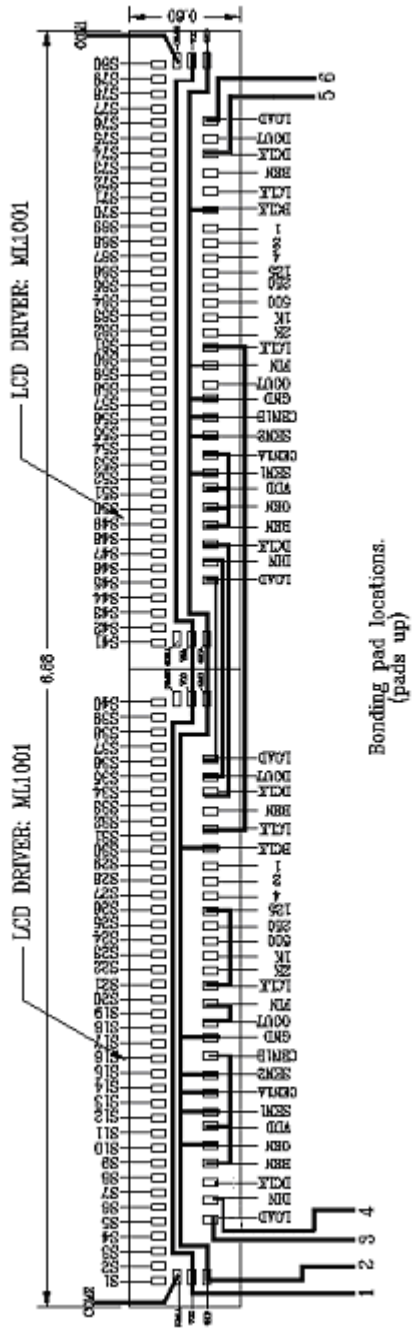


Pin	Pin Name
1	VDD
2	GND
3	LOAD
4	DIN
5	DCLK
6	FIN
7	CHECK

Note : If External 32 KHz Clock Signal is available, designer can turn off Internal Oscillator to save power.

Note : Pin LOAD and Pin CHECK shall be connected together if the flip-chip assembly is in good condition. Hence, Pin CHECK can be served for qualifying the flip-chip assembly quality.

ML1001D-2U Standard Application



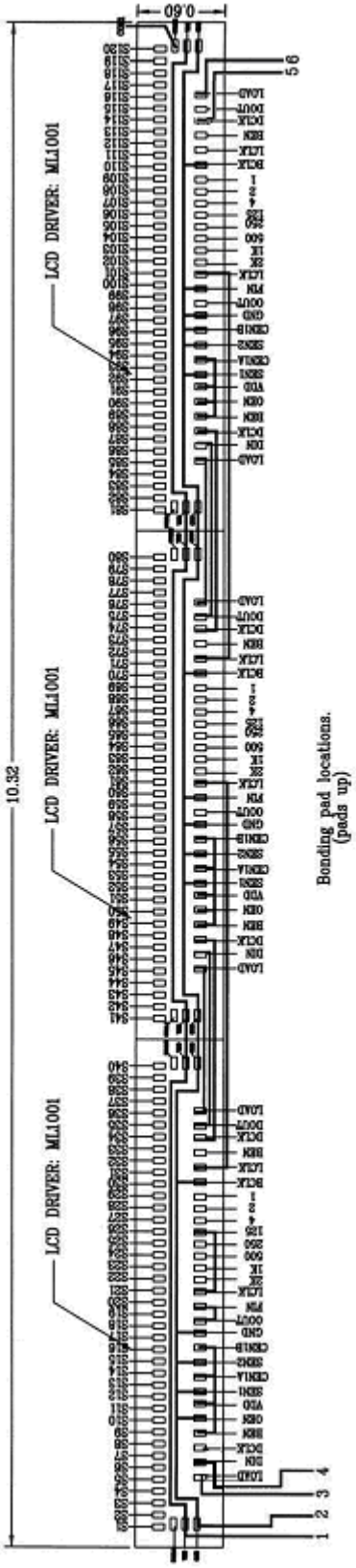
Pin	Pin Name
1	VDD
2	GND
3	LOAD
4	DIN
5	DCLK
6	CHECK

Note :

Chip 1 Pad Coordinate shall follow "Table of Pad Location".
Chip 2 Pad Coordinate shall be calculated as follow :

Chip 2 X-Coordinate = Chip 1 X-Coordinate + 3,440um
Chip 2 Y-Coordinate = Chip 1 Y-Coordinate

ML1001D-3U Standard Application



Pin	Pin Name
1	VDD
2	GND
3	LOAD
4	DIN
5	DCLK
6	CHECK

Note :

Chip 1 Pad Coordinate shall follow "Table of Pad Location".
Chip 2 Pad Coordinate shall be calculated as follow :

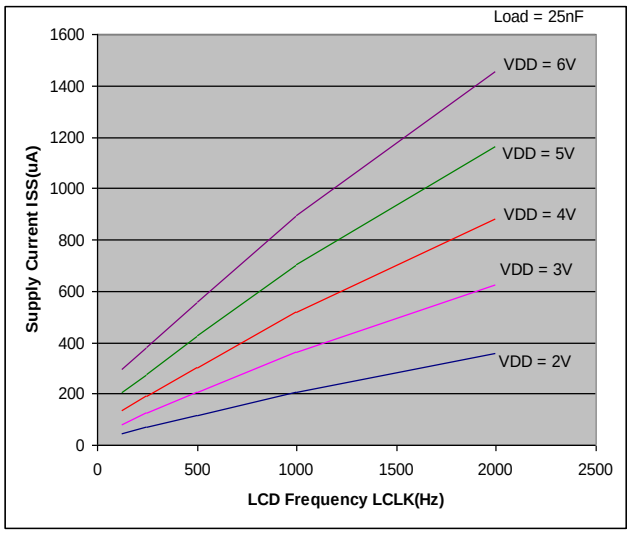
Chip 2 X-Coordinate = Chip 1 X-Coordinate + 3,440um
Chip 2 Y-Coordinate = Chip 1 Y-Coordinate

Chip 3 Pad Coordinate shall be calculated as follow :

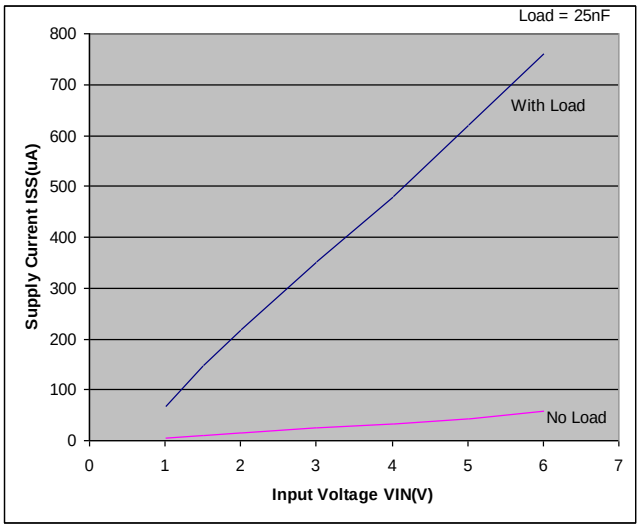
Chip 3 X-Coordinate = Chip 1 X-Coordinate + 6,880um
Chip 3 Y-Coordinate = Chip 1 Y-Coordinate

❖ *Typical Characteristics*

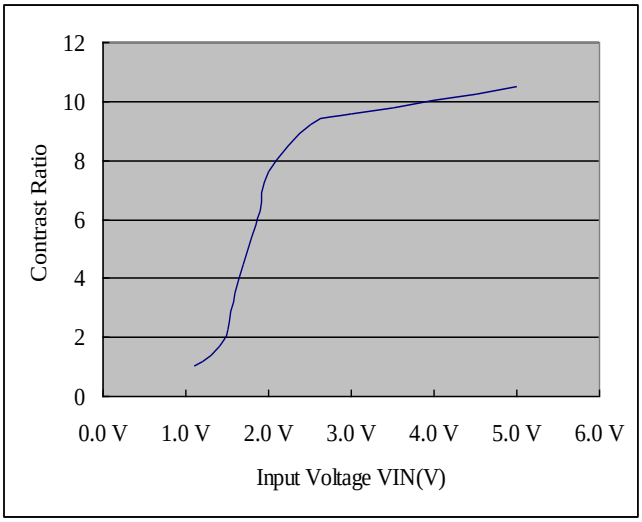
1) Supply Current vs. Frequency of LCLK



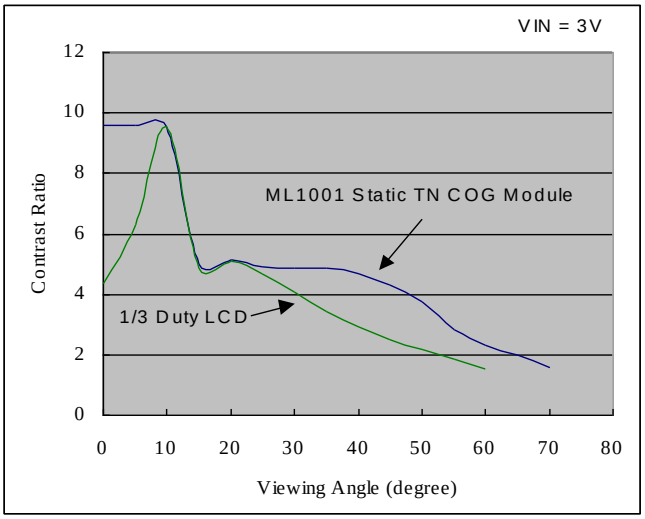
2) Supply Current vs. Input Voltage



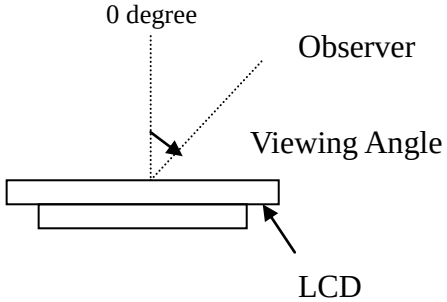
3) Example of Contrast Ratio vs. Input Voltage



4) Example of Contrast Ratio vs. Viewing Angle



Note: 1. Contrast ratio of LCD shall vary from the Liquid Crystal used.
2. Contrast ratio of 1/3 Duty LCD is shown on graph 4 for comparison only.
3. The viewing angle is measured from the normal of LCD as shown below.



❖ *Application Note*

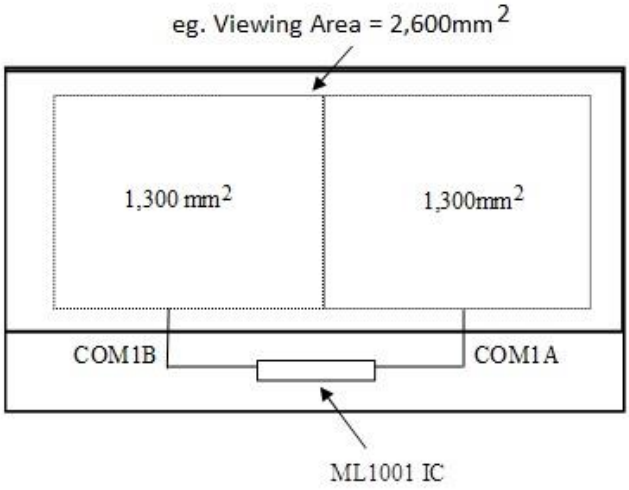
1. To ensure LCD module work properly, DCLK has to connect to 2nd ML1001D IC for ML1001D-2U configuration as shown on page 10, or 3rd ML1001D IC for ML1001D-3U configuration as shown on page 11.

2. To ensure the good flip-chip assembly quality, we suggest flip-chip bonding house add a "CHECK" pin for each COG module as shown on the section of "Application Example". Pin "LOAD" and Pin "CHECK" shall be connected together if the flip-chip assembly is in good condition. The measured resistance between Pin "LOAD" and Pin "CHECK" shall not more than 5 kohm.

3. The resistance of ITO glass shall between 15 ohm/□ to 25 ohm/□.

4. Each Common (ie. COM1A and COM1B) shall not cover more than 2,000 mm^2 area. In case the Viewing area of LCD has to be more than 2,000 mm^2, more common output has to be used.

Example :



Note : COM1A and COM1B shall cover half of the Viewing Area (ie. Area = 1,300mm^2)
Each Common shall not connect to each other.

I/O PIN ITO Resistance Limitation

Pin Name	ITO Resistance
BEN, OEN, SEN1, CEN1A, SEN2, CEN1B	No Limitation
LOAD, DIN, DCLK, OOUT, FIN, LCLK, 2K, 1K, 500, 250, 125, 4, 2, 1, BCLK, LCLK, DOUT	< 1kΩ
VDD, GND	< 200Ω